

cro-fluidic applications as well as nanostructured percolation media. The hollow funnels can also serve as “nanocrucibles” for metal alloy production, which permit the containment and handling of very small amounts of metals. The latter would be of interest to the field of combinatorial synthesis, for instance, as potential micro/nano arrays for solid-state synthesis.

Experimental

The deposition experiments were conducted in an ASTeX 5010 Microwave Plasma reactor on various substrates including graphite, molybdenum, and titanium. A thin film of gallium is spread on the substrate. On top of the gallium film molybdenum powder purchased from Alfa Aesar (3–7 μm, 99.95 % purity) was dusted (1–15 % molybdenum to gallium atomic ratio). The setup was then exposed to 18 % CH₄/H₂ plasma at 1100 W microwave power and 40 torr reactor pressure for 1 h. The experiments were started by first striking the hydrogen plasma followed by introducing the methane gas. The experiments were shut down by turning off the methane gas followed by turning off the hydrogen gas supply. The heating of the substrate is solely due to the plasma, with no independent substrate heating. The temperature of the substrate was measured to be 800–850 °C by an optical pyrometer. Experiments to synthesize conical structures were performed using CH₄/H₂ only. In other experiments to control the morphology, the feed gases were dosed with 5 sccm of O₂ to 18 sccm of CH₄ and 100 sccm of H₂ at various stages of the growth process as required. For example, to synthesize funnels, oxygen was introduced right from the start of the experiment for about 30 min followed by turning off the oxygen gas supply. No other parameters were changed. The described structures were not observed on the as-synthesized samples. A layer of molybdenum–gallium alloy was observed as the top-most layer on the sample, which might have segregated during the shut down procedure. This could be avoided by temperature-controlled shut down, not possible with the reactor used. When the plasma is turned off, there is a sudden fluctuation in the temperature, as there is no substrate heating. This top layer was removed by gently tapping the sample, thus exposing the underneath carbon structures which are all over the substrate. The synthesized structures are analyzed using a JEOL JSM 5310 scanning electron microscope operated at 25 kV and a JEOL 2010F transmission electron microscope operated at 200 kV. For TEM analysis the structures formed on the substrate were transferred onto a holey carbon grid.

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30 nm Channel Length Pentacene Transistors**

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Organic thin film transistors (OTFTs) are being developed for applications in smart tags and display drivers. Dramatic advances in the performance of organic semiconductors have been achieved in recent years and have brought their performance, in terms of field-effect mobility, to levels comparable with amorphous silicon.^[1] A critical dimension in a TFT is the channel length L (the distance between the source and drain electrodes). Typically, transistors are fabricated with L of the order of tens of micrometers using optical lithography or by deposition through a stencil.^[1] Studies of TFTs with much smaller L ^[2–11] have been motivated by the desire to increase both the device speed and the saturation current, the highest current that the transistor delivers at a given gate voltage.

As early as 1987, Turner-Jones et al. demonstrated an organic transistor with a 50 nm channel length, which was defined by using shadowed deposition of Au on a tilted substrate.^[2] The transistor worked in the electrochemical mode, i.e., by modulation of the conductivity of polyaniline through electrochemical doping/dedoping. In 1993, Franssila et al. demonstrated the first sub-100 nm organic field-effect transistor.^[3] Anisotropic etching was used to fabricate nanoscale oxide pillars that served as the lift-off masks for defining the channel. Solution-coated polythiophene was used as the semiconductor. However, the characteristics of the transistors were poor, exhibiting only minor gating effects.

More recently, Collet et al. used electron beam lithography to define channels as small as 30 nm.^[4,7,8] The channels were fabricated directly on top of evaporated films of small molecules such as sexithiophene. Rogers et al. combined near-field photolithography with microcontact printing and shadow masking to demonstrate complementary inverter circuits from organic transistors with $L = 100$ nm.^[5] A phthalocyanine and

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an oligothiophene were used as the n- and p-type semiconductors respectively. Granstrom and Frisbie used electron-beam lithography to fabricate sexithiophene transistors with channel lengths between 300 and 500 nm.^[6,9] Austin and Chou successfully fabricated 70 nm channel length polythiophene transistors using nanoimprint lithography.^[10] Finally, Zaumseil et al. used high-resolution rubber stamps to define channels down to 150 nm and fabricated pentacene transistors.^[11]

In all previous work, the characteristics of the TFTs have degraded when the channel length was decreased below 100 nm. For example, the CNRS group reported that for channel lengths below 200 nm the drain current (I_{SD}) no longer follows the usual shape for the output characteristics of a TFT,^[1] but it varies in a superlinear function with drain voltage (V_{SD}).^[7] This was attributed to ballistic transport of charge between the source and the drain, as opposed to transport dominated by field effects at the semiconductor–dielectric interface. The I_{SD} versus V_{SD} characteristics were analyzed in terms of Fowler–Nordheim tunneling, implying that charge injection at the source–sexithiophene interface was the rate limiting step in current transport through the transistor. Superlinear I_{SD} versus V_{SD} characteristics observed by the Minnesota group in transistors with 300–500 nm channel length were attributed to poor charge injection.^[9] Analysis of the temperature dependence of the current versus voltage characteristics revealed an effective contact resistance that was dependent on the drain as well as the gate voltage. Superlinear I_{SD} versus V_{SD} characteristics were also observed by the Princeton group^[10] for devices with 70 nm channel lengths and were attributed to “punch-through”. This is an effect that occurs at high current densities, where the formation of space charge in the channel prevents the saturation of I_{SD} . From these reports, it is not clear whether these effects represent an inherent limitation in the performance of sub-100 nm organic transistors or they were just associated with the particular set of materials used and details of the device geometry (e.g., insulator thickness relative to channel length).

In this communication, we report the fabrication of pentacene transistors with channel lengths down to 30 nm. Advances in sample fabrication have allowed us to vary channel lengths and widths over large ranges with precision on the 10-nanometer scale. In contrast to previous work, we demonstrate graceful scaling of the I_{SD} versus V_{SD} characteristics as a function of channel length and width. We use pentacene as the organic semiconductor because of its high mobility, which has made it the standard molecule for benchmarking organic transistor structures.^[1]

The transistor fabrication is described in the experimental section. In brief, a three step electron beam lithography process allowed the fabrication of channels with lengths L down to 30 nm, as shown in Figure 1a. Pt, which due to its high work function is expected to be a good hole injector, was used for the source and drain electrodes. The oxide underneath the channel was 30 nm thick, and an appropriately patterned layer of photoresist allowed the electrical isolation of each transistor (Fig. 2a).

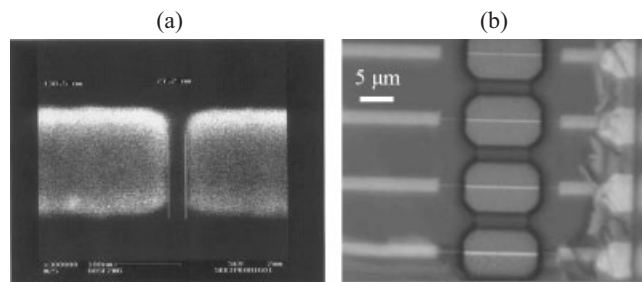


Fig. 1. a) Source and drain electrodes with $L=27$ nm and $W=130$ nm. b) $6\ \mu\text{m} \times 10\ \mu\text{m}$ windows in the photoresist used for the isolation of the transistors (four transistors shown).

The characteristics of a transistor with $L=30$ nm and $W=100$ nm, operated in the (hole) accumulation regime, are shown in Figure 2a. Reversible behavior with negligible hysteresis was observed when V_{SD} and V_{SG} were kept between 0 and -2 V and 0 and -4 V, respectively (the I_{SD} vs. V_{SD} curves shown in Figure 2a are superimposed “up” and “down” voltage scans). Beyond these values, the devices would frequently exhibit hysteretic behavior and breakdown. The I_{SD} versus

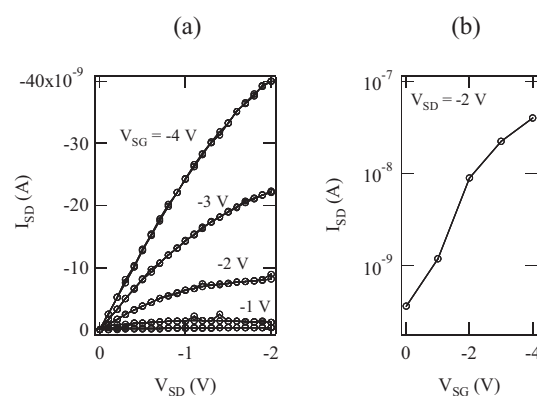


Fig. 2. a) I_{SD} vs. V_{SD} characteristics and b) transfer characteristics for a pentacene transistors with $L=30$ nm and $W=100$ nm.

V_{SD} curves show the behavior expected from a p-channel TFT, being initially linear with V_{SD} and then saturating (saturation is not observed for the higher V_{SG} since V_{SD} was limited to below -2 V). These curves show no evidence for ballistic transport or channel “punch-through”, meaning that such effects are not an inherent limitation of sub-100 nm transistors.

The field-effect mobility was calculated from the linear regime of the I_{SD} versus V_{SD} curves and was found to be $2 \times 10^{-2}\ \text{cm}^2\ \text{V}^{-1}\ \text{s}^{-1}$.^[12] This is of the same order of magnitude as in pentacene TFTs with $L=20\ \mu\text{m}$ prepared under the same conditions.^[13] The low value of the mobility in the latter devices was attributed to the small size of the crystallites. Pentacene deposited in high vacuum, at a rate of $0.1\ \text{\AA}\ \text{s}^{-1}$, on SiO_2 room-temperature substrates yields polycrystalline films with crystallites on the order of 100 nm.^[13] For transistors with $L=30$ nm, one might therefore expect single-crystal performance, i.e., a field-effect mobility of the order of $1\ \text{cm}^2\ \text{V}^{-1}\ \text{s}^{-1}$.^[13] The lower field-effect mobility measured in

our nanoscale TFTs might be due to the fact that they employ bottom contacts. It is known that when pentacene is deposited on a SiO₂ substrate with metal electrodes, it tends to form smaller grains in the neighborhood of the electrodes, with detrimental effects in the field-effect mobility.^[13,14] If this is the case, a two order of magnitude increase in the field-effect mobility of our devices may be possible by increasing the grain size. A detailed investigation of the morphology of pentacene in the channel region is currently underway.

The transfer characteristics of the same transistor are shown in Figure 2b. An ON/OFF ratio $I_{\text{ON/OFF}}$ of 10^2 is observed. This is small compared to $I_{\text{ON/OFF}}$ measured in pentacene transistors with micrometer size channels, which is typically of the order of 10^5 (state-of-the-art pentacene transistors show $I_{\text{ON/OFF}}$ in excess of 10^7).^[1] The small $I_{\text{ON/OFF}}$ in the nanoscale devices appears to be due to a large OFF current. Namely, the conductivity of pentacene in the channel was found to be 2 orders of magnitude larger than that in micrometer scale devices prepared from the same pentacene batch. This might be due to accumulated charge at the contacts, which plays an increasingly important role as the channel length decreases. It should be noted that the leakage current through the gate oxide was too low (< 6 pA) to account for the small ON/OFF ratio. Also, positive V_{SG} bias did not result into gating.

In contrast to devices with large channels, where averaging over many grains with different size and orientation takes place, nanometer-scale devices based on polycrystalline materials such as pentacene are expected to show significant variation in their performance. In Figure 3, histograms indicating the spread in I_{SD} at $V_{\text{SD}} = -2$ V and $V_{\text{SG}} = -4$ V are shown for

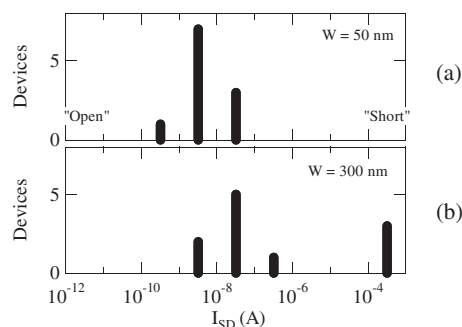


Fig. 3. Histograms displaying the number of devices that exhibit an I_{SD} in a certain current range, vs. I_{SD} , for $V_{\text{SD}} = -2$ V, $V_{\text{SG}} = -4$ V. a) $L = 30$ nm, and $W = 50$ nm; b) $L = 30$ nm, and $W = 300$ nm. Electrically open devices had an $I_{\text{SD}} < 10$ pA (no such device shown in this figure) while in shorted devices, the current was limited by the source measure unit to 0.5 mA.

TFTs with $L = 30$ nm and two different values of channel width. For TFTs with $W = 50$ nm, 7 out of 11 show I_{SD} between 1 and 10 nA. One device shows a current which is an order of magnitude lower, while 3 devices show an I_{SD} that is an order of magnitude higher. When the channel width is increased to 300 nm, 5 out of 11 devices show an I_{SD} between 10 and 100 nA, exhibiting the expected scaling with W . Two TFTs showed an order of magnitude lower I_{SD} , one showed an I_{SD} that was on order of magnitude higher, while three

others had characteristics consistent with a metallic short between the electrodes. We also fabricated devices with $W = 30$ nm, and for these we had occasional difficulties with discontinuous electrodes (3 out of 11 TFTs were electrically open), while TFTs with W larger than 300 nm showed an increasing fraction of shorts (5 out of 11 for $W = 500$ nm and $L = 30$ nm were shorts). Studies of the morphology of pentacene in the channel region will help better understand the spread in the TFT performance and establish strategies to reduce it.

In conclusion, we have fabricated pentacene transistors with 30 nm channel length. Their current–voltage characteristics exhibited the behavior expected for p-channel TFTs. Typical field-effect mobilities were of the order of 10^{-2} cm² V⁻¹ s⁻¹, similar to values measured in transistors with larger channel lengths and bottom contacts. This work shows that it is possible to realize functional organic transistors with channel lengths down to 30 nm, and that their characteristics scale gracefully with channel length and width down to these small values. The value of the field-effect mobility implies that there may be room for a two orders of magnitude increase in performance, which can be gained by better understanding growth of pentacene in the channel region.

Experimental

The transistors were fabricated on low resistivity (3–5 mΩ cm), single-side polished (100) silicon wafers. In order to remove any surface defects on the wafer, a 1 μm thick wet oxide was grown thermally and stripped in hydrofluoric acid. The oxide growth was then repeated, and windows of 80 μm × 55 μm were opened with photolithography. The oxide within the windows was removed by etching and a 30 nm thick layer of dry oxide was grown to serve as the gate dielectric. This procedure allows for good gate coupling by means of a thin gate oxide underneath the transistor channel, while the rest of the wafer is covered with a thicker oxide, decreasing the occurrence of shorts. The source and drain electrodes, consisting of 30 nm thick Pt with a 3 nm Ti adhesion layer, were then defined by electron-beam lithography, using the Leica VB6 system with a PMMA bilayer resist. The adhesion layer was buried into the oxide by means of a brief CF₄ plasma etch just before the metal deposition, in order to ensure that the first monolayer of pentacene came in contact with Pt. Ordinarily it is difficult to fabricate two electrodes separated by a very narrow channel using electron beam lithography, because the proximity effect leads to unwanted exposure of the resist in the channel area [15]. In order to avoid this problem, we patterned our devices using three separate e-beam patterning and deposition steps [16]. The first step involved the deposition of alignment marks, while the second and third steps defined separately the source and drain electrodes. In this way, definition of the channel length is limited only by alignment accuracy, approximately 10 nm. We fabricated channels with lengths L down to 30 nm and widths W from 30 to 500 nm. An example of source and drain electrodes is shown in Figure 1a.

In order to electrically isolate the devices from each other, we fabricated an isolated region of pentacene on each transistor, with no leakage path between devices. This was achieved by coating the wafer (prior to pentacene deposition) with a 1.5 μm thick layer of photoresist and patterning it to define windows of 6 μm × 10 μm centered around the channels of the individual transistors (Fig. 1b), and also around the contact pads. Following an ion-milling step used to clean the channel area, we then deposited a pentacene layer, typically 25 nm thick, by thermal evaporation under high vacuum ($\sim 10^{-6}$ torr) at a rate of about 0.1 Å s⁻¹, with the substrate held at room temperature. Since the photoresist was much thicker than the evaporated pentacene layer, it caused a discontinuity in the latter, defining an isolated pentacene island on each channel. After completion of the fabrication, the devices were moved through air and tested under high vacuum in a Desert Cryogenics probe station.

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Highly Efficient and Thermally Stable Electro-optic Polymer from a Smartly Controlled Crosslinking Process**

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Organic second-order nonlinear optical (NLO) polymers have received increasing interests due to their potential for applications in high-speed electro-optic (EO) devices with very broad bandwidths and low drive voltages, and can be made with cost-effective fabrication processes.^[1] Recently, prototype EO modulators exhibiting large EO coefficients and low drive voltages have been demonstrated by using guest–host poled polymers with these highly efficient chromophores.^[1a,2] However, these materials often suffer from low thermal stability and poor solvent resistance during the multilayer fabrication process.^[1–3] Thus, it is highly desirable to covalently incorporate chromophores into polymer networks and harden the matrix through crosslinking reactions to improve both their thermal and mechanical properties.^[2,4]

Although the approach of lattice hardening has been well illustrated in numerous examples for relatively small-sized and inactive chromophores, such as dispersed red (DR) and diethylamino nitrostilbene (DANS), applying this approach to highly polarizable chromophores usually results in a significant reduction of 20–40% in EO activity.^[2] This is because highly efficient chromophores often possess much larger dipole moment and bulkier sizes than DR and DANS. In the poling process, the poling field not only has to compete with the strong dipole–dipole interaction but also the steric hindrance caused by chromophore–polymer chain entanglements. Usually, the poling of conventional NLO thermoset polymers is achieved through a simultaneous lattice hardening and poling process. As a result, the lattice hardening significantly reduces the rotational flexibility of the bulky dye moieties due to the increase in glass-transition temperature (T_g) and interchain entanglements of the polymers.^[2,5] This inhibits chromophore reorientation under the poling field, resulting in a significantly decreased poling efficiency and the so-called “nonlinearity-stability trade-off”. Therefore, the possibility to realize the full potential of organic NLO materials is severely limited. For example, the EO coefficient of a poled polyurethane thermoset was found to possess a much lower EO coefficient (r_{33}) value than what was obtained from a guest-host materials using the same chromophore (36 versus 57 pm V^{-1} at $1.06 \mu\text{m}$).^[6a]

In addition, several other deficiencies also exist that limit the employment of conventional crosslinking polymers for EO devices. For example, high temperatures, needed for curing these thermoset polymers, often cause decomposition of highly polarizable chromophores.^[6] Moreover, the condensation-type crosslinking reactions, represented by the polyurethane and epoxy crosslinking schemes, usually involve the reactions of O–H and/or N–H units. It is well known that the vibrational overtones of these polar O–H/N–H groups at 1400–1600 nm contribute significantly to the absorption optical loss at the operational wavelength of telecommunication, such as 1550 nm.^[2,5,6] These polar groups can also act as nucleophiles which will attack the electron acceptors in highly efficient chromophores.^[2,6] On the other hand, the addition-type crosslinking systems, such as acrylic and cinnamoyl polymers also generate another type of harsh chemical environments: the very reactive free radicals generated during polymerization will destroy highly polarizable chromophores even more rapidly.^[7]

Recently, we have found that the incorporation of the dendritic moiety into highly efficient Cheng–Larry–Dalton (CLD)-type chromophores allow them to be efficiently poled in both guest–host and side-chain polymers and afford exceptionally high r_{33} values, up to 97 pm V^{-1} .^[8–9] This demonstrates that the site-isolation effect can be employed to improve the poling efficiency of high $\mu\beta$ chromophores in linear thermoplastic polymers. Although these results are quite encouraging, the dendron-attached chromophores are much bulkier than the unsubstituted ones. As a result, we have encountered another challenge when we were trying to perform lattice

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